REMARKS

Claim Rejections Under 35 USC §103

Claims 24-36 have been rejected under 35 USC 103(a) as being unpatentable over the admitted prior art in view of Lee et al. (U.S. Patent No. 5,796,586).

In response to the 35 USC §103 rejections, the claims have been amended. In addition, the Examiner is asked to consider the arguments to follow.

The amended claims are directed to a board-on-chip semiconductor package 62 (Figure 6B). As shown in Figure 6B, the BOC package 62 includes a substrate 56 comprising a first surface 44 with a pattern of conductors 48, an opposing second surface 46 with a die attach area 50, and a wire bonding opening 64 extending through the substrate 56 from the first surface 44 to the second surface 46. In addition, the package 62 includes a first solder mask 80A having openings 82 for attaching solder balls 88 to the conductors 48, and an opening 84 (Figure 3C) for wire bonding to the conductors 48. The package 62 also includes a second solder mask 80B having an opening 86 (Figure 3D) on the die attach area 50.

As also shown in Figure 6B, the package 62 includes a semiconductor die 16 placed face down (circuit side down) through the opening 86 in the second solder mask 80B, and attached directly to the substrate 56 in the die attach area 50. An adhesive layer 72 (Figure 6A) attaches the face of the die 16 directly to the substrate 56. The package 62 also includes wires 94 placed through the wire bonding opening 64 in the substrate 56, and bonded to bonding pads on the face of the die 16, and to bonding pads 52 (Figure 6A) on the conductors 48. In addition, solder balls 88 are placed through the openings 82 in the first solder mask 80A, and attached to ball bonding pads 54 (Figure 6A) on the conductors 48. As also shown in Figure 6B, an encapsulating resin 90 is molded over the die 16, and over the second

solder mask 80B. Further, a glob top 92 can be placed over the wires 94, and in the wire bonding opening 64 to protect the wire bonds.

Argument

MPEP 2142, 2143 set forth the three basic criteria for establishing a prima facie case of obviousness under 35 USC §103(a). First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success in obtaining the claimed invention based upon the references relied upon by the Examiner. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicants would firstly argue that there is no suggestion or motivation in the references or the art to combine the admitted art with Lee et al. The admitted art discloses a board-on-chip package (10-Figure 1A) in which the die (16) is bonded face down to the solder mask (22). Lee et al. discloses a substrate board (200-Figure 7) having conductive traces (202) and a solder mask 218' which is configured to protect the conductive traces (column 7, lines 56-58). However, there would be no incentive to use the Lee et al. configuration in the admitted art board-on-chip package (10), because there are no conductive traces on the die attach area to protect. Rather, the die (16) is bonded face down to the substrate (12), and wire bonded to conductors (18) which are location on the opposing side of the substrate (12).

The present invention recognizes that an open die attach area provides improved adhesion for a die bonded face down to a substrate. The Examiner is privy to this teaching by virtue of the present disclosure. However, the prior art

including Lee et al. does not contain this teaching which is the primary motivation for the combination of the admitted art and Lee et al.

Applicants would secondly argue that the prior art does teach or suggest all of the claim limitations of the amended claims. One limitation not taught by the cited prior art is stated in each of the amended independent claims. In particular, as stated in independent claim 24 the package includes "a second mask (80B-Figure 7) covering the second surface (46-Figure 3A) except in a die attach area (50-Figure 4A) defined by an opening (86-Figure 4A) through the second mask having a second outline substantially matching the first outline".

Figure 7 of Lee et al. was cited as teaching this feature. However, the solder mask (218') in Lee et al. must leave the tips of the conductive traces exposed for wire bonding (column 8, lines 6-7). In addition, the die must be spaced from these tips in order to provide room for the wires that are wire bonded to the die and to the tips. Accordingly the die attach (204) in Lee et al. would need to be significantly larger than the outline of the die. With the present arrangement the solder mask 80B can comprise a high adhesion resist (e.g., Taiyo PSR-4000 resist described at page 10 lines 15-18 of the present specification and at column 7, lines 66-67 of Lee et al.). In addition, the solder mask 80B has a larger surface area for adhesion with the encapsulant.

Another feature not taught by the admitted art or Lee et al. and claimed in amended dependent claims 26, 33 and 36 is the use of a "filled adhesive" or "filled epoxy" in combination with the open die attach area. Such a filled adhesive has improved thermal conductivity characteristics. The open die attach area and the filled adhesive in combination improve heat transfer between the die and the substrate.

Conclusion

In view of the above arguments and amendments, favorable consideration and allowance of claims 24-36 is respectfully requested. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

Dated this 12th day of January 2001.

Respectfully submitted:

Stephen A. Gratton
Registration No. 28,418
Attorney for Applicants

2764 S. Braun Way
Lakewood, CO 80228
Telephone: (303) 989-6353
FAX (303) 989-6538

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

"Express Mail" Mailing Label Number EK 235 815 275 US
Date of Deposit: January 12, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents, Box CPA, Washington, D.C. 20231.

January 12, 2001
Date of Signature

Stephen A. Gratton, Attorney for Applicants

MARKED VERSION TO SHOW CHANGES TO AMENDED CLAIMS

24. (twice amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, [and] a plurality of conductors and ball bonding pads on the first surface, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline and a face on the bonding opening bonded directly to the second surface; [and having a first outline;]

a first mask on the first surface comprising a plurality of via openings [to] aligned with the ball bonding pads;

a second mask [substantially] covering the second surface except in a die attach area defined by [including] an opening [there] through the second mask having a second outline substantially matching the first outline; [to define an open die attach area on the second surface; and]

an adhesive layer between the die and the substrate in the [open] die attach area bonding the [die directly] face to the second surface; and

a plurality of wires placed through the bonding opening and wire bonded to the die and to the conductors.

25. (twice amended) The package of claim 24 further comprising an encapsulating material at least partially encapsulating the die and the second mask.

26. (twice amended) The package of claim 25 wherein the adhesive layer comprises a filled adhesive. [substrate includes a wire bonding opening and the die is aligned with the wire bonding opening, bonded circuit side down to the second surface, and wire bonded to the conductors.]

27. (twice amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors [and ball bonding pads] on the first surface comprising ball bonding pads and wire bonding pads, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline, the die comprising a [circuit side] face on the bonding opening bonded to the second surface;

[, and aligned with the bonding opening;]

a first mask on the first surface comprising a plurality of via openings aligned with [selected] the ball bonding pads [on the conductors] and a first opening exposing [selected] the wire bonding pads;

[on the conductors;]

a second mask substantially covering the second surface [and including] comprising a second opening [there through] having a second outline substantially matching the first outline to define an open die attach area on the second surface;

an adhesive layer between the die and the substrate in the open die attach area bonding the [circuit side of the die] face to the second surface; and

a plurality of wires in the bonding opening wire bonded to the die and to the wire bonding pads.

[conductors.]

28. (twice amended) The package of claim 27 further comprising a glob top in the bonding opening and on the first surface at least partially encapsulating the wires.

29. (twice amended) The package of claim 27 wherein the first mask and the second mask comprise a photoimageable [dielectric] material.

30. (twice amended) A semiconductor package comprising:

a substrate having a first surface, [and] a second surface and a bonding opening there through;

a plurality of conductors on the first surface comprising a plurality of ball bonding pads;

a first mask on the first surface comprising a plurality of via openings to the ball bonding pads;

a semiconductor die having a face on the bonding opening attached directly to the second surface;

[in electrical communication with the conductors, the die having a first outline;]

a second mask [substantially] covering the second surface [and including] except in a die attach area defined by an opening [there] through the second mask having [a second] an outline substantially matching that of the face;

[the first outline to define an open die attach area on the second surface permitting the die to be bonded directly to the second surface; and]

a plurality of solder balls in the via openings bonded to the ball bonding pads; and

a plurality of wires placed through the bonding opening and bonded to the die and to the conductors.

31. (twice amended) The package of claim 30 further comprising an encapsulating resin on the second surface at least partially encapsulating the die.

32. (twice amended) The package of claim 30 further comprising a plurality of wire bonding pads on the conductors wire bonded to the wires and a second opening in the first mask exposing the wire bonding pads.

[a wire bonding opening through the substrate aligned with the die and a plurality of wires wire bonding the die to the conductors.]

33. (twice amended) The package of claim 30 further comprising [an] a filled adhesive layer attaching the die to the substrate in the open die attach area.

34. (twice amended) A semiconductor package comprising:

a substrate comprising a first surface, an opposing second surface and a wire bonding opening from the first surface to the second surface;

a plurality of conductors on the first surface [, each conductor] comprising [a] wire bonding pads and [a] ball bonding pads;

a first mask on the first surface comprising a plurality of via openings aligned with [selected] the ball bonding pads [on the conductors] and a first opening exposing [selected] the wire bonding pads;
[on the conductors;]

a semiconductor die aligned with the wire bonding opening and bonded [circuit side] face down to the second surface, the die having a first outline;

a second mask substantially covering the second surface and including an opening there through having a second outline substantially matching the first outline to define an open die attach area on the second surface;

an adhesive layer between the die and the substrate in the open die attach area bonding the die directly to the second surface;

a plurality of wires placed through the wire bonding opening and bonded to the die and to the wire bonding pads; and

an encapsulating resin on the second surface at least partially encapsulating the die.

35. (twice amended) The package of claim 34 further comprising a glob top in the wire bonding opening at least partially encapsulating the wires.

36. (twice amended) The package of claim 34 wherein the adhesive layer comprises a filled epoxy.
[material selected from the group consisting of filled epoxy, unfilled epoxy, acrylics and polyimide.]